DEPARTMENT OF TECHNICAL EDUCATION

DIPLOMA COURSE IN ELECTRONICS & COMMUNICATION ENGINEERING

FIFTH SEMESTER

VHDL LAB

Subject Code: 506

Contact Hrs. / week: 6 **Contact Hrs. / Sem: 96 HRS**

Necessary equipment needed for the Lab

1. VHDL Simulator Software
2. Synthesis software
3. FPGA/CPLD training Kit
4. Experiment boards in which programmed FPGA/CPLD can be used

Graded Exercises

Write Logic diagram and execute the following programs using

VHDL simulator software and FPGA/CPLD Trainer kit

1. Write VHDL code to realize all the logic gates
2. Full Adder (using Data flow, Structural,& Behavioral modelings)
3. Full Subtractor
4. BCD to Seven Segment Decoder
5. Binary to Gray Converter (4-bit)
6. 4-Bit Comparator (Ex: 7485)
7. Decimal to Binary Encoder
8. 3:8 Decoder (Ex: 74LS138)
9. 4:1 Multiplexer
10. 1:4 De-multiplexer
11. Parity Generator
12. 4 Bit Parallel Adder
13. D Flip flop
14. JK Flip flop
15. T Flipflop
16. BCD Counter
17. Modulo N Counter
18. 4-Bit Universal Shift Register
19. Up Down Counter (4-bit)
20. 4-bit ALU with 2 logical & 2 arithmetic operations

Text Book

1. VHDL Primer by J. Bhaskar
2. VHDL by Douglas Perry
3. HDL Programming VHDL and Verilog by Nazeih M Botros - Dreamtech Publications

	Scheme of valuation	
1	Record	5
2	Writing any two Programs	30
3	Program Simulation & Downloading to kit (any one program)	30
4	Result	15
5	Viva - Voce	20
	Total	100